REMARKS

File History

In the Office action of 6/12/2003, the following rejections, objections were made:

> Claim 11 was indicated to contain allowable subject matter.

> Claims 1, 2, 9, 10, 12, 13 were rejected under 35 USC §102(a) as being fully anticipated by Chao et al (US 6,291,030 based on an application filed 12/21/1999).

> Claims 3-8, 14-40 were rejected under 35 USC §103(a) as being obvious over Chao et al in further view of Liu et al (US 6,211,040 based on an application filed 9/20/1999).

> Claims 1-40 were rejected (or objected to) under 35 USC §112 for indefiniteness.

Summary of Current Response

Claim 11 is re-written into independent form.

Claims 1, 12, 17-25, 28-30 and 35-36 are amended.

Claims 41-58 are newly introduced.

The specification is amended.

Arguments are presented concerning the applied art and its proposed combination.

The correspondence address of record is amended.

Applied Art

The Examiner is correct in finding that Chao '030 discloses an HDP-CVD step wherein the sputter to deposition ratio is made very low, "under 0.1 and more preferably around 0.0." as stated at col. 3, line 43. This low S/D ratio is established during the second of three (3) successive HDP-CVD steps which respectively form three inter-metal dielectric

layers: 403, 501 and 601 on top of metal lines 401 of Fig. 6. This low S/D ratio (<0.1) is established **for the purpose of intentionally inducing formation of voids 503** in the inter-metal dielectric and of thereby reducing the effective dielectric constant (k) of the inter-metal dielectric. (See Chao col. 3, line 45.)

During the first of the 3 successive HDP-CVD steps of Chao, the S/D ratio is made relatively high (>0.2 per col. 3, line 30) so as to provide "very good step coverage over the metal lines 401" (Chao col. 3, lines 31-32.) During the third of the 3 successive HDP-CVD steps, the S/D ratio is again made relatively high (>0.4 per col. 3, line 56). Nowhere does Chao teach or suggest that a very low S/D ratio should be established for the purpose of filling in trenches of different aspect ratios with a silicon oxide. In other words, Chao does not teach to use a near-zero S/D ratio for all purposes. Instead Chao teaches to do so only when forming voids in an intermetal dielectric (IMD) for purpose of reducing dielectric constant (k).

Liu '040 was cited as the secondary reference for combining with Chao. Liu '040 teaches away from allowing voids to form (see Summary col. 2, lines 66-67). Liu '040 teaches keeping the E/D ratio in the range 0.12 to 0.15 (col. 4, line 46).

Arguments

Claim 1 is amended here to clarify that the claimed method is directed to depositing a silicon oxide into trenches defined in a semiconductor substrate, where at least two of the trenches are of different aspect ratios, and where ions are used to sputter etch a portion of the reactively formed silicon oxide during the deposition so as to fill the trenches with the formed silicon oxide. Chao '030 fails to teach or suggest the use of an E/D ratio of about 0.07 or less during the filling of trenches with different aspect ratios. Therefore Claim 1 is patentably distinguishable over Chao '030. Liu '040 is not combinable with Chao because Liu '040 teaches away.

Claims 2, 9, and 10, depend from Claim 1 and are therefore patentably distinguishable over Chao '030 for the same reasons applied to Claim 1.

Claim 12 has been amended to clarify that the claimed product has at least two trenches of different widths and that the trenches are filled with an oxide formed from the recited process. Chao '030 fails to teach or suggest the use of an E/D ratio of about 0.07 or less during the filling of trenches with different widths. Therefore Claim 12 is patentably distinguishable over Chao '030. Claim 13 depends from Claim 12 and is therefore patentably distinguishable over Chao '030 for the same reasons applied to Claim 12.

With respect to Claims 3-8 and 14-40, the outstanding Office action admits that Chao fails to teach use of the recited (1) oxygen-to-silane ratios, (2) total gas flow and/or (3) high frequency bias power. The Office action proposes to cure this deficiency by combining Chao with Liu '040. No rationale is given for *why* the ordinary artisan would chose to combine Chao with Liu. Instead it is asserted that it would have been within the scope of capability of the ordinary artisan to combine Chao with Liu.

Applicants respectfully disagree that it is legally permissible to combine Chao with Liu in the manner proposed. Liu '040 teaches away from Chao and vise versa. Liu '040 teaches keeping the E/D ratio in the range 0.12 to 0.15 (col. 4, line 46). Liu '040 teaches to avoid forming voids (col. 2, lines 66-67). Chao contrastingly teaches to intentionally form voids in the middle one of 3 deposited layers of dielectric. In other words, Chao teaches to use a low E/D ratio only when intentionally creating voids in a middle one of 3 dielectric layers. Neither of Chao and Liu teaches to use a specific E/D ratio for the purpose of filling trenches of differing aspect ratios and/or trenches of differing widths. Thus, even if Chao and Liu could be somehow combined and their contradictions resolved, the combination would fail to fully replicate the recited subject matter.

With respect to Claim 29, note that recited combination includes helium.

Referring to page 9, line 27 of the specification, note that the disclosed HDP-CVD process allows for more uniform planarization of the oxide-filled trenches by way of CMP and acid etch. In the one recited example, post-acid-etch surfaces 36, 38 are within about 600Å of the planarized tops 40 of the adjacent silicon regions 16. This supports Claim 53.

Request for Examination and Allowance

Examination is respectfully requested for the amended application. In view of the above, it is respectfully submitted that all of previous Claims 1-40 and all of new Claims 41-58 are in condition for allowance.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-2257 for any matter in connection with this response, including any fee for extension of time and/or fee for additional claims, which may be required.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 12, 2003.

[signature] 8-12-2003

Attorney for Applicant(s) Date of Signature

Respectfully submitted,

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APPENDIX A: CLEAN COPY OF NEW OR AMENDED CLAIMS

1. A method of depositing silicon dioxide into trenches defined in a semiconductor substrate, where at least two of the trenches are of different aspect ratios, said depositing method comprising:

(a) using oxygen and silane gases to reactively form silicon dioxide for deposition into said different trenches of the substrate;

(b) using ions to sputter etch a portion of the formed silicon dioxide during the deposition so as to fill the trenches with the formed silicon dioxide; and

(c) controlling the etch and the deposition of the silicon dioxide such that a nonzero etch to deposition ratio of about 0.07 or less is established during the filling of said different trenches.

2. The method of Claim 1 further comprising controlling the deposition and the etch such that the etch to deposition ratio is 0.025 or less.

3. The method of Claim 1 further comprising using an oxygen to silane ratio of 1.3 or less.

4. The method of Claim 1 further comprising using a total gas flow of the oxygen, the silane, and an inert gas of 625 standard cubic centimeters per minute or less.

5. The method of Claim 1 further comprising using a total gas flow of the oxygen, the silane, and an inert gas of 500 standard cubic centimeters per minute or less.

6. The method of Claim 1 further comprising using a high frequency bias signal power of 2000 watts or less.

7. The method of Claim 1 further comprising using a high frequency bias signal power of 1500 watts or less.

8. The method of Claim 1 further comprising the act of doping the silicon dioxide during deposition.

9. The method of Claim 1 further comprising the act of depositing the silicon dioxide over an electrically conductive layer used as an interconnect.

10. The method of Claim 9, wherein the electrically conductive layer is metal.

11. A method of depositing silicon dioxide over a semiconductor substrate, comprising:

using oxygen and silane gases to deposit silicon dioxide over the substrate;

using ions to etch a portion of the deposited silicon dioxide during the deposition;

controlling the etch and the deposition of the silicon dioxide such that an etch to deposition ratio is 0.07 or less depositing the silicon dioxide over a layer of silicon nitride, the silicon nitride being formed over a layer of polycrystalline silicon;

polishing the silicon dioxide to expose a top surface of the silicon nitride; and

etching the silicon dioxide such that a top surface of the etched silicon dioxide is below a top surface of the layer of polycrystalline silicon.

12. An integrated circuit structure comprising silicon dioxide filling at least two trenches of differing widths, where the trench-filling silicon dioxide of said at least two trenches is the product of a method comprising:

(a) using oxygen and silane gases to reactively form the silicon dioxide;

(b) using ions to etch a portion of the formed silicon dioxide; and

controlling the etch and the deposition of the silicon dioxide such that a nonzero etch to deposition ratio of about 0.07 or less is established during the filling of said at least two trenches of differing widths.

13. The integrated circuit of Claim 12, wherein the etch to deposition ratio is 0.025 or less.

14. The integrated circuit of Claim 12, wherein using oxygen and silane gases comprises using an oxygen to silane ratio of 1.3 or less.

15. The integrated circuit of Claim 12, wherein using oxygen and silane gasses comprises using a total gas flow rate of the oxygen, the silane, and an inert gas, the total gas flow rate being 625 standard cubic centimeters per minute or less.

16. The integrated circuit of Claim 12, wherein using oxygen and silane gasses comprises using a total gas flow rate of the oxygen, the silane, and an inert gas, the total gas flow rate being 500 standard cubic centimeters per minute or less.

17. The integrated circuit of Claim 12, wherein the ions used during deposition of the silicon dioxide are subjected to a high frequency bias signal power of 2000 watts or less.

18. The integrated circuit of Claim 12, wherein the ions used during deposition of the silicon dioxide are subjected to a high frequency bias signal power of 1500 watts or less.

19. A method of depositing silicon dioxide into trenches defined in a semiconductor substrate, where at least two of the trenches are of different aspect ratios, said depositing method comprising:

(a) using silane gas, oxygen gas, and an inert gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less, and wherein the total flow rate of the silane, oxygen, and inert gasses is 500 standard cubic centimeters per minute or more; and

(b) controlling a bias signal which affects a sputter etch action of the inert gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075.

20. The method of Claim 19, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

21. The method of Claim 19, wherein the bias signal is controlled to have a power of 2000 watts or less.

22. The method of Claim 19, wherein the bias signal is controlled to have a power of 1500 watts or less.

23. The method of Claim 19, wherein a total flow rate of the silane, oxygen, and inert gasses is 625 standard cubic centimeters per minute or less.

24. An integrated circuit structure comprising silicon dioxide formed in plural trenches where at least a first trench is at least twice as wide a second of the trenches, the silicon dioxide having been deposited by a deposition method comprising:

(a) using silane gas, oxygen gas, and an inert gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less, and wherein the total flow rate of the silane, oxygen, and inert gasses is 500 standard cubic centimeters per minute or more; and

(b) controlling a bias signal which affects a sputter etch action of the inert gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075.

25. The integrated circuit of Claim 24, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

26. The integrated circuit of Claim 24, wherein the signal has a power of 2000 watts or less.

27. The integrated circuit of Claim 24, wherein the signal has a power of 1500 watts or less.

28. The integrated circuit of Claim 24, wherein a total flow rate of the silane, oxygen, and inert gasses is 625 standard cubic centimeters per minute or less.

29. A method of depositing silicon dioxide into trenches defined in a semiconductor substrate, where at least two of the trenches are of different aspect ratios, said depositing method comprising:

(a) using silane gas, oxygen gas, and helium gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less; and

(b) controlling a bias signal which affects a sputter etch action of the helium gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075.

30. The method of Claim 29, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

31. The method of Claim 29, wherein the signal has a power of 2000 watts or less.

32. The method of Claim 29, wherein the signal has a power of 1500 watts or less.

33. The method of Claim 29, wherein a total flow rate of the silane, oxygen, and helium gasses is 625 standard cubic centimeters per minute or less.

34. The method of Claim 29, wherein the total flow rate is 500 standard cubic centimeters per minute or less.

35. An integrated circuit structure comprising silicon dioxide formed in plural trenches where at least a first trench is at least twice as wide a second of the trenches, the silicon dioxide having been deposited by a deposition method comprising:

(a) using silane gas, oxygen gas, and a helium gas to reactively form, deposit, and resputter the silicon dioxide, wherein a ratio of oxygen inflow rate to silane inflow rate is 1.7 or less; and

(b) controlling a bias signal which affects a sputter etch action of the helium gas to thereby establish an etch-to-deposition ratio for the formed silicon dioxide which is less than 0.075.

36. The method of Claim 35, wherein the ratio of oxygen to silane inflow rates is 1.3 or less.

37. The method of Claim 35, wherein the signal has a power of 2000 watts or less.

38. The method of Claim 35, wherein the signal has a power of 1500 watts or less.

39. The method of Claim 35, wherein a total flow rate of the silane, oxygen, and helium gasses is 625 standard cubic centimeters per minute or less.

40. The method of Claim 35, wherein the total flow rate is 500 standard cubic centimeters per minute or less.

41. The depositing method of Claim 1 wherein a first of said trenches is at least twice as wide as a second of said trenches.

42. The depositing method of Claim 1 wherein a first of said trenches has a width in the range of about 1800Å to 3300Å and a second of said trenches has a width in the range of about 6600Å to 8800Å.

43. The method of Claim 1 and further comprising:

(d) overfilling said at least two of the trenches with the deposited silicon dioxide; and

(e) using chemical mechanical polishing (CMP) to remove at least a portion of the overfilling silicon dioxide.

44. The method of Claim 43 and further wherein said at least two of the trenches have silicon nitride at top portions thereof and said CMP removal stops at the silicon nitride top portions of said at least two trenches.

45. The method of Claim 1 wherein the used ions include helium.

46. A method of using high-density plasma chemical-vapor deposition (HDP-CVD) to deposit silicon oxide on a semiconductor-containing substrate having trenches defined therein, where the trenches include those of different aspect ratios, at least one trench having a relatively high depth-to-width aspect ratio equal to or greater than 2.5 and at least a second trench having a depth-to-width aspect ratio which is comparatively smaller, said HDP-CVD method comprising:

(a) applying one or more electromagnetic fields to an ionized plasma containing oxygen, silane, and an inert gas where the oxygen and silane of the plasma can reactively

combine to form first silicon oxide for deposition on the semiconductor-containing substrate; and

(b) controlling at least one of:

(b.1) the oxygen-to-silane ratio in the plasma,

(b.2) a first of the electromagnetic fields, and

(b.3) total input gas flow for supplying said oxygen, silane, and inert gas to said plasma,

to thereby establish a nonzero etch-to-deposition ratio (E/D ratio) condition of about 0.07 or less where said E/D ratio can be defined as a difference in thickness of net deposited silicon oxide with said first electromagnetic field turned on and off divided by the thickness of net deposited silicon oxide with said first electromagnetic field turned off.

47. The HDP-CVD method of Claim 46 wherein the ionized plasma further contains a sputter etch agent which can sputter etch at least a portion of the deposited first silicon oxide; and

(b.3a) the total gas inflow of the oxygen, silane and the sputter etch agent is about 625 standard cubic centimeters per minute (sccm) or less.

48. The HDP-CVD method of Claim 46 wherein the first silicon oxide includes silicon dioxide.

49. The HDP-CVD method of Claim 46 wherein the first silicon oxide includes phospahate silica glass.

50. The HDP-CVD method of Claim 46 wherein the comparatively smaller aspect ratio of the second trench less than about 1.

51. The HDP-CVD method of Claim 50 wherein the first trench has a width in the range of about 1800Å to 3300Å.

52. The HDP-CVD method of Claim 46 wherein the inert gas includes helium.

53. A monolithically integrated device having a semiconductor-containing substrate and plural trenches defined to extend into at least one layer of the device to substantially same depths, where at least a first and second of said same-depth trenches respectively have different widths, the width of the second trench being at least twice the width of the first trench, said integrated device being further characterized by:

(a) said same depth trenches of different widths are each filled with a silicon oxide deposited by way of high-density plasma chemical-vapor deposition (HDP-CVD) to substantially same heights above said substantially same depths to thereby provide a substantially planar set oxide-filled trenches upon which other layers of material are founded.

54. The integrated device of Claim 53 wherein:

(b) the heights of said oxide-filled trenches lie adjacent to silicon regions.

55. The integrated device of Claim 54 wherein:

(b.1) the heights of said oxide-filled trenches are within about 600Å of reference top surfaces of the adjacent to silicon regions.

56. The integrated device of Claim 54 wherein:

(b.1) the heights of said oxide-filled trenches are defined at least by chemical mechanical polishing (CMP).

57. The integrated device of Claim 56 wherein:

(b.2) the heights of said oxide-filled trenches are further defined by an acid etch carried out after said chemical mechanical polishing (CMP).

58. The integrated device of Claim 57 wherein:

(b.3) the heights of said oxide-filled trenches, after said acid etch, are within about 600Å of reference top surfaces of the adjacent to silicon regions.

APPENDIX B: AMENDMENTS TO SPECIFICATION – MARKED-UP VERSION

Paragraph beginning on line 17 of page 9 has been amended as follows:

Referring again to FIG. 1, embodiments of the invention result in the difference between the layer 20 thickness over surface 22 and the layer 20 thickness over surface 26 is less than when using known HDP-CVD processes. Following deposition, in one embodiment layer 20 is polished using conventional CMP to expose the top surface of silicon nitride layer 18. Such CMP results in surface 32 over trench 10 and surface 34 over trench 12. Layer 20 is further etched using a conventional hydrofluoric acid etch to produce surface 36 over trench 10 and surface 38 over trench 12. In one case surfaces 36 [46],38 are approximately 600 Å below top surface 40 of polycrystalline silicon layer 16.

Paragraph beginning on line 1 of page 10 has been amended as follows:

Skilled artisans will appreciate that the specific embodiments disclosed herein are illustrative, and that many variations are possible. Embodiments are not confined to depositing silicon dioxide or silicon substrates. For example, embodiments may include an HDP-CVD process for phosphate silica glass (PSG), which may be used as the premetal layer dielectric. Embodiments may also be used for intermetal dielectric layer processes. Therefore, the scope of patent protection sought [the invention] is defined by the claims appended hereto [following claims].

APPENDIX C: AMENDMENTS TO SPECIFICATION – CLEAN VERSION

Paragraph beginning on line 17 of page 9 has been amended as follows:

Referring again to FIG. 1, embodiments of the invention result in the difference between the layer 20 thickness over surface 22 and the layer 20 thickness over surface 26 is less than when using known HDP-CVD processes. Following deposition, in one embodiment layer 20 is polished using conventional CMP to expose the top surface of silicon nitride layer 18. Such CMP results in surface 32 over trench 10 and surface 34 over trench 12. Layer 20 is further etched using a conventional hydrofluoric acid etch to produce surface 36 over trench 10 and surface 38 over trench 12. In one case surfaces 36,38 are approximately 600 Å below top surface 40 of polycrystalline silicon layer 16.

Paragraph beginning on line 1 of page 10 has been amended as follows:

Skilled artisans will appreciate that the specific embodiments disclosed herein are illustrative, and that many variations are possible. Embodiments are not confined to depositing silicon dioxide or silicon substrates. For example, embodiments may include an HDP-CVD process for phosphate silica glass (PSG), which may be used as the premetal layer dielectric. Embodiments may also be used for intermetal dielectric layer processes. Therefore, the scope of patent protection sought is defined by the claims appended hereto.